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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/551,187	ZENG, JUN	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2002*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *76-104* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *76-104* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's amendment and petition filed on 2/27/02, in which Claims 1-75 were canceled. New pending claims 76-104 have been are currently pending.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

*** Claim 89 is objected for including a grammatical error of "...comprises are arranged...", and should be --...are arranged...--.

Specification

*** Specification page 1, line 1, is objected as current status of parent application 09/107,721 should be updated to include --U.S. Patent No. 6,104,062--.

Claim Rejections - 35 USC § 112

1. Claims 77-78, 82-83,86,91-93,97,102-104 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

* Claims 77 and 78 are incomplete and indefinite as they depends on cancelled claim 52.

* Re claims 82,83, the limitation of "...the at least resistivity-lowering body..." is lacking proper antecedent basis and improper, since base claim 76 recites "...resistivity-lowering bodies...", as plural.

* Re claims 86 and 97, the limitation of "...adjacent the at least one device active region" is lacking proper antecedent basis. . Base claim 76 does not mention forming at least one device active region.

* Re claims 91-93, the limitation of "...wherein forming the at least one device active region..." lacks proper antecedent basis. Base claim 76 does not mention forming at least one device active region.

* Re claims 102-104, the limitation of "...wherein forming the at least one device active region..." lacks proper antecedent basis. Base claim 94 does not mention forming at least one device active region.

Claim Rejections - 35 USC § 102

2. Claims 76,82-86,91-92, 94-97,102,103 are rejected under 35 U.S.C. 102(e)/(a) as being anticipated by Okabe et al (5,663,096).

Re base claim 94, Obake teaches a method for forming a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity, the method (at Figs 1-3; col 3, line 52 through col 5) comprising at least the steps of : in the substrate, forming a drain layer 2,1 of a first polarity; in a first surface, forming one or more well regions 4 above the drain layer 2 and comprising dopants of a second and opposite polarity; in the first surfaces and in said well regions 4, forming source regions 6 of dopants of the first polarity, the source regions 6 laterally spaced form each other (Figs 1; col 3, line 52 through col 4); forming gate regions 10 over portions of the well regions 4 between the source regions 6 and the drain layer 2; and in the second surface of the substrate 1 forming one or more resistivity-lowering bodies 26 extending from the second surface of the substrate into interior portions of the semiconductor substrate 1 (Figs 1,2B; col 4, line 20 through col 5, line 31), the resistivity-lowering bodies formed in the concave recessed into the substrate comprising a material of different than the semiconductor substrate 1 and having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate 1, inherently (col 5, lines 57 through col 6, line 11), wherein the material comprising Ti-Ni-Au layers, wherein the Au layer is a contact layer. Re claim 95, wherein an electrical contact layer 26 on the second surface of the semiconductor substrate is electrically connected to the at least one resistivity lowering body recessed into the concaves. Re claim 96, wherein the resistivity lowering body of titanium, nickel, gold is inherently having an electrical resistivity less than about 10^{-4} Ohms/cm (col 6, lines 1-11). Re claim 97, wherein as shown in figure 1 a proportion is greater than about 0.4 percent. Re claims 102,103, MOSFET and IGBT are mentioned at col 6, lines 47-57.

Re base claim 76, Okabe teaches a method for forming a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity, the method (at Figs 1-3; col 3, line 52 through col 5) comprising at least the steps of : in the first surface, forming a plurality of source regions 6 of dopants of one polarity, the source regions all electrically connected together; in the substrate below the source regions 6, forming a drain layer 2,1 of dopants of the same polar as the source regions 6; between the source regions 6 and the

drain layer 2, forming well regions 4 of dopants of the opposite polarity to define channels between the source regions 6 and the drain layer 2; forming gate regions 10 over the channel and between the source regions and the drain layer 2, the gate regions 10 electrically connected together; forming a pattern of recesses extending from the second surface of the substrate into interior portions of the semiconductor substrate 1, the recesses located at chosen positions, and having chosen shapes and chosen depths in the substrate 1 due to the granularity of the grindstone (Figs 1,2B; col 4, line 20 through col 5, line 48); and forming resistivity-lowering bodies in the recesses concaved into the substrate, the resistivity-lowering bodies 26 comprising a material having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate, inherently (col 5, lines 57 through col 6, line 11), wherein the material comprising Ti-Ni-Au layers, wherein the Au layer is a contact layer. Re claim 82, wherein the electrode layer 26 including an electrical contact layer 26 and the resistivity-lowering bodies are formed on the second bottom surface of the semiconductor substrate. Re claim 83, wherein the resistivity-lowering body 26 is filled in the associated recess 22 (Figs 1,2B-2C). Re claim 84, wherein the electrode layer 26 includes a multilayer electrode so as to comprise a barrier layer lining in at least one recess (Fig 1,2C; col 6, lines 1-10). Re claim 85, wherein the resistivity lowering body of titanium, nickel, gold is inherently having an electrical resistivity less than about 10^{-4} Ohms/cm (col 6, lines 1-11). Re claim 86, wherein as shown in figure 1, a proportion of the semiconductor substrate and the recesses is greater than about 0.4 percent. Re claims 91,92, MOSFET and IGBT are mentioned at col 6, lines 47-57.

Claim Rejections - 35 USC § 103

3. Claims 79-81,87,88-90,93,98,99-101,104 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okabe et al (5,663,096) taken with Iwai (4,597,166) and Yamane (JP-62243332).

Obake teaches a method (at Figs 1-3; col 3, line 52 through col 5) for forming a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity, as applied above to claims 76,82-86,91-92, 94-97,102,103.

Obake teaches forming a plurality of recesses in the second bottom surface of the semiconductor substrate, but lack mentioning to form the recesses in grid pattern of cutting

trenches, repeated pattern, trapezoidal pattern, array of recesses (79-81,88-90,99-101). Re claims 87,98, wherein the recess depth is greater than 25 percent of the semiconductor substrate.

However, Iwai teaches forming a plurality of recess into the second bottom surface of the semiconductor substrate, wherein the recesses comprising a repeated pattern, a grid pattern of cutting trenches, trapezoidal pattern, array of recesses (Figs 2A-7; col 4, line 40 through col 5). Yamane teaches grinding the second bottom surface oft eh semiconductor substrate 1 to form a plurality of recesses having a repeated pattern, a grid pattern of cutting trenches, and an array of recesses (Figs 1-3, English abstract). Re further claims 87-98, as shown in Iwai, the depth of the recesses is greater than 25 percent of the semiconductor substrate (Figs 2A-7).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the recesses of Okabe to have the recesses in repeated pattern, in grid pattern of cutting trenches, trapezoidal pattern, array of recesses, as taught by Iwai and Yamane. This is because of the desirability to form the recesses having diversity shapes including repeated pattern, in grid pattern of cutting trenches, trapezoidal pattern, array of recesses so that the electrode can be firmly adhered to the semiconductor substrate.

Re claims 93,104, the references including Okabe lack forming a microprocessor using such semiconductor device. However, it is official notice that using the semiconductor device to form a microprocessor is well known in the semiconductor art. Therefore, it would have been obvious to one of ordinary skill in the art at least because of the desirability to form a computer for processing and storing data, wherein the semiconductor device is a low power consumption device.

4. Claims 76,79,82-87,91,94-98,102 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo (JP-62063472) taken with Pruniaux et al (3,823,352).

Re base claim 76 and 94, Kubo teaches a method for forming a semiconductor device comprising a semiconductor substrate having a lowered effective electrical resistivity, the method (at Fig 1, English abstract) comprising at least the steps of : in the first surface, forming a plurality of source regions 4a of dopants of one polarity in the well regions 3a-3c, the source regions all electrically connected together; in the substrate below the source regions 4a-4d, forming a drain layer 2/1/12 of dopants of the same polar as the source regions 4; between the

source regions 4 and the drain layer, forming well regions 3a-3c of dopants of the opposite polarity in the first surface above the drain layer to define channels between the source regions 4 and the drain layer; forming gate regions 6a-6b over the channel and over portions of the well regions 3 between the source regions and the drain layer (Fig 1), and the gate regions 6 electrically connected together; forming a pattern of recesses 11 in the substrate in the other side of the gate 6, and extending from the second surface of the substrate into interior portions of the semiconductor substrate 1,2,12, the recesses located at chosen positions, and having chosen shapes and chosen depths in the substrate; and forming a layer 10 of resistivity-lowering bodies in the recesses concaved into the substrate and extending into interior portions of the semiconductor substrate, the layer 10 of resistivity-lowering bodies comprising a conductive material different than the semiconductor substrate, and having an electrical resistivity lower than an electrical resistivity of the semiconductor substrate, inherently. Re claim 79, wherein the pattern of recesses is repeated for a plurality of connected devices (Fig 1). Re claims 82 and 95, wherein the electrode layer 10 including an electrical contact layer and the resistivity-lowering bodies are formed in the recesses and on the second bottom surface of the semiconductor substrate (Fig 1). Re claim 84, wherein a barrier layer 10 or 12 is lining the recesses. Re claims 86 and 97 wherein as shown in figure 1, a proportion of the semiconductor substrate and the recesses is greater than about 0.4 percent. Re claims 87,98, wherein as shown in Figure 1, the recess extending into the substrate greater than about 25 percent. Re claims 91 and 102, wherein a MOSFET is mentioned at page 347, right column, last paragraph.

Re claims 76,94,83, Kubo teaches forming the electrode layer 10 in the recess, but appears lacking to have the resistivity-lowering bodies formed by filling the recesses. Re claims 85,96, wherein the resistivity of the resistivity lowering is less than about 10^{-4} Ohms/cm.

However, Pruniaux teaches (at Figs 1-3; col 4, line 1 through col 5) forming in the recess at least one lowering body 16 comprising a material having an electrical resistivity lower than that of the semiconductor substrate, wherein the material comprising platinum or platinum silicide, and forming a gold or silver contact layer by electroplating thereon (col 5, lines 40-47), wherein the resistivity lowering body of platinum, gold, silver is inherently having an electrical resistivity less than about 10^{-4} Ohms/cm.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the electrode of Kubo by filling the pattern of recesses with an electrical conductive metal as taught by Pruniaux. This is because of the desirability to provide effective thermal conduction, and to reduce substantially parasitic source resistance (in Pruniaux, col 5, lines 44-48; col 2, lines 9-15), wherein ON resistance of the device is reduced (English abstract of Kubo).

5. Claims 92-93 and 103-104 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo (JP-62063472) taken with Pruniaux et al (3,823,352), as applied to claims 76,79,82,83,85-87,91,94-98,102 above, and further of Okabe (5,663,096).

The references including Kubo and Pruniaux teach a method for forming a semiconductor device as applied to claims 76,79,82,83,85-87,91,94-98, and 102 above.

The references teach the device as a MOSFET, but lacks to mention to use the device in forming an IGBT (claims 92,103) or a microprocessor (claims 93,104).

However, Okabe et al teach (at col 6, lines 47-57) to apply the method in forming a device of MOSFET or IGBT.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the method in forming the device of MOSFET or IGBT as combinatively taught by Okabe and Pruniaux. This is because of the desirability to form high voltage devices having low ON-resistance. Using these devices for forming a microprocessor for a computer, as well known in the semiconductor art, would have been obvious to one of ordinary skill in the semiconductor art because of the desirability to form a computer for processing and storing data and information, wherein these devices are low power consumption.

6. Claims 80-81,88-90,99-101 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kubo (JP-62063472) taken with Pruniaux et al (3,823,352), as applied to claims 76,79,82,83,85-87,91,94-98,102 above, and further of Iwai (4,597,166).

The references including Kubo and Pruniaux teach a method for forming a semiconductor device as applied to claims 76,79,82,83,85-87,91,94-98, and 102 above.

The references including Kubo and Pruniaux teach forming a plurality of recesses in the second bottom surface of the semiconductor substrate, but lack mentioning to form the recesses in grid pattern of cutting trenches, trapezoidal pattern, array of recesses (79-81,88-90,99-101).

However, Iwai teaches forming a plurality of recess into the second bottom surface of the semiconductor substrate, wherein the recesses comprising a repeated pattern, a grid pattern of cutting trenches, trapezoidal pattern, array of recesses (Figs 2A-7; col 4, line 40 through col 5).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the recesses of Kubo by forming the recesses in repeated pattern, in grid pattern of cutting trenches, trapezoidal pattern, array of recesses, as taught by Iwai, Kubo and Pruniaux. This is because of the desirability to form the recesses having various shapes including repeated pattern, in grid pattern of cutting trenches, trapezoidal pattern, array of recesses so that the electrode body can be formed into the recesses, thereby providing effective thermal conduction, and reducing substantially parasitic source resistance (in Pruniaux, col 5, lines 44-48; col 2, lines 9-15), wherein ON resistance of the device is thus reduced (English abstract of Kubo).

Response to Arguments

7. Applicant's arguments have been fully considered but they are not persuasive, and to are also moot in view of the new ground(s) of rejection.

It is noted claim 94 merely recites "...one or more resistivity-lowering bodies extending from the second surface of the substrate into interior portions of the semiconductor substrate...", not a "...forming a patterning of recesses extending...into interior portions of the semiconductor substrate...". Okabe still clearly teaches such limitations.

Yamane shows an array of recesses formed by grinding and lapping, not randomly (Figs 1-3).

****

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F from 8:30 Am to 4:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Oacs-15

Michael Trinh
Primary Examiner